A LOW VOLTAGE RF RECEIVER FOR DIGITAL SATELLITE RADIO

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ABSTRACT

An integrated low voltage RF receiver for the Digital Satellite Radio is presented. It uses innovative solutions for critical blocks such as LNA, IF buffer, VCO, etc., and includes power supply regulators at 2.4 V.

The circuit has been integrated in a high performance 20-GHz silicon bipolar technology and correctly operates with an external power supply varying from 2.7 V to 5.5 V.

INTRODUCTION

The receiver is based on a dual conversion architecture with a single IF filter. It operates on a QPSK modulated signal whose minimum level is set to -92 dBm.

To reduce common mode noise coming from the substrate and the supply lines, a fully differential architecture has been adopted and proper bias circuits have been designed. The differential approach also improves stability, minimizes the risk of unwanted oscillation in high-gain blocks, and increases linearity that is a critical performance in a QPSK receiver.

The circuit provides an overall gain of 120 dB and a noise figure of 5 dB. Moreover, the RF oscillator achieves a phase noise of –99 dBc/Hz at 100 kHz frequency offset.

The bit error rate with the minimum input signal level is lower than 10^{-4}.

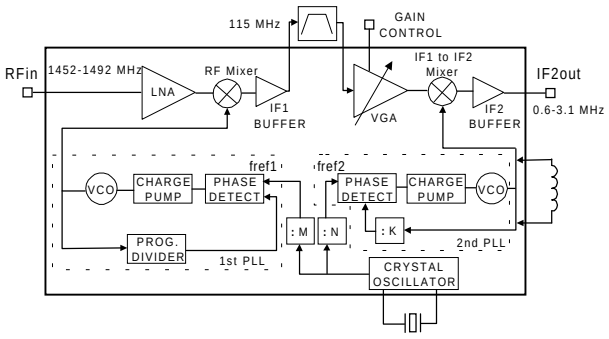

Figure 1 : Block diagram of the receiver

SYSTEM DESCRIPTION

A block diagram of the proposed receiver is shown in Fig.1. It includes all the basic building blocks from the RF front-end to the baseband interface. The receiver transforms a 1.5-GHz RF signal in a 2-MHz baseband signal for the external A/D converter and channel decoder.

The first stage is an LNA that works in the 1.452-1.492 GHz band. Then, the RF signal is down converted by a double balanced mixer to a first 115-MHz intermediate frequency (IF). The IF signal is delivered to an external channel filter by a high linear IF buffer. The insertion loss of this filter is around equal to 23 dB. An overall gain of 50 dB is achieved from the RF input to the IF buffer output. To compensate for the input power variations, a VGA (Variable Gain Amplifier) has been included in the receiver chain. Finally, a second conversion and a baseband buffer provide a 1 V peak-to-peak signal for the external A/D converter.

The receiver includes two PLLs for the first and second downconversion. The PLL in the

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

first conversion uses a fully integrated VCO, a programmable divider, and a digital phase comparator. The reference oscillator, running at 14.72 MHz, is made up of an integrated amplifier and an external quartz. It is also used as reference in the second PLL. The VCO in the second PLL is at 117-MHz fixed frequency and uses an external inductor.

MAIN BLOCK DESCRIPTION

A. Low Noise Amplifier

A schematic of the differential low noise amplifier (LNA) is shown in Fig. 2 [1]. Feedback is used to achieve an input resistance very close to the source resistance. Thanks to it, the input impedance is well controlled and both a high return loss and a low noise figure have been achieved.

The LNA is based on the cascode differential stage, Q1-Q4, and is followed by the common collectors Q5 and Q6. Resistances R_F perform a shunt-shunt feedback configuration. To increase gain while avoiding output swing reduction, pump resistances R_A have been included which set the bias current in Q1 and Q2 higher than that in the load resistances R_C.

By inspection, it is easy to find that a good approximation for the differential input resistance, R_i, is

$$R_i \approx 2\frac{R_F}{g_{m1,2}R_C} \qquad (1)$$

where $g_{m1,2}$ is the transconductance of the emitter-coupled pair Q1-Q2.

To provide input impedance matching, R_i has been set equal to the differential source resistance, R_s.

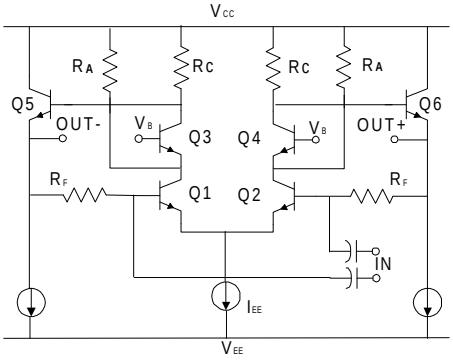

Figure 2 : Low noise amplifier

The LNA voltage gain, A_V, is given by

$$A_V = g_{m1,2} R_C \qquad (2)$$

Thanks to the PTAT bias current in Q1 and Q2, A_V is set by the ratio between poly resistances and emitter areas, and Ri is proportional to a poly resistance.

Neglecting some minor high frequency contributions and setting the optimum transconductance value in Q1 and Q2, the noise factor is

$$F_{opt} = 1 + \frac{r_{b1,2}}{R_S} + \frac{R_S}{R_F} + \frac{1}{\sqrt{\beta_F}} \qquad (3)$$

B. IF Buffer

To increase linearity, efficiency and to provide an accurate output impedance matching, a class AB feedback configuration has been used for the IF buffer. The circuit is shown in Fig. 3. It is basically a differential emitter follower stage, Q1, Q2, in which transistors Q3-Q6 perform a feedback loop and capacitor C_C provides frequency compensation. Thanks to the feedback loop, the inherent output resistance, $2/g_{m1,2}$ is reduced by the loop gain $g_{m3,4}\cdot R_C$ so achieving an accurate transfer gain and hence a high linearity. Moreover, due to the very low output resistance, a good impedance matching can be provided by including resistances R_{E1}.

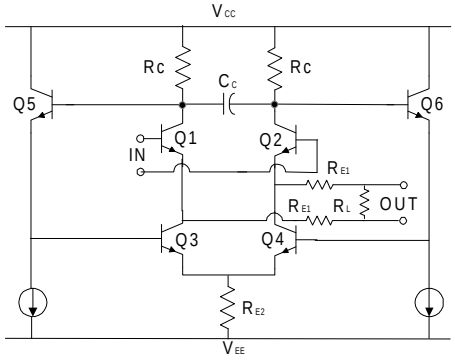

Figure 3 : IF buffer

As far as power conversion efficiency, η, is concerned, simple calculations give

$$\eta = \frac{1}{2}\frac{V_{oMAX}}{V_{CC} - V_{EE}} \qquad (4)$$

where V_{OMAX} is the maximum output level. In our design V_{OMAX} and the power supply are 0.5 V and 2.4 V, respectively, and η is around equal to 30%.

C. Voltage Controlled Oscillator

The RF oscillator is shown in Fig. 4. It uses integrated spiral inductors and standard base-collector varactors [2]. The peak detector (made up of Q5-Q6 and capacitor C3) together with the error amplifier perform a low frequency feedback loop which sets the current in Q3 and Q4 and hence the oscillation amplitude to the reference voltage V_R.

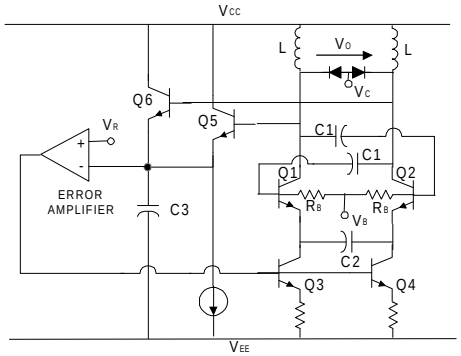

Figure 4 : Voltage controlled oscillator

To overcome the limitation on the tuning range, three selectable oscillators with different values of varactor capacitances have been implemented. Thanks to them, a wide frequency range, even in worst case conditions, is achieved.

The finite Q value of the inductors and the low frequency noise of the error amplifier (which is folded on the oscillation frequency) are the dominant contribution to the phase noise. With a proper oscillation amplitude and an accurate design of the low frequency loop, a phase noise of -99 dBc/Hz at 100 kHz has been achieved.

D. Voltage regulator

A simplified schematic of the voltage regulator is shown in Fig. 5. The regulator is composed of three main blocks: a PTAT current generator Q1-Q4, a band-gap voltage generator Q5-Q7 and an operational amplifier that includes NPN transistor Q8 and feedback resistances R5 and R6. Current I_{PTAT} is set regardless the value of V_{CE} and R_B, provided that V_{CE} is greater than 2 V_{BE}. Terminal V_{CE} is used as chip enable. The regulator provides 2.4 V power supply and correctly woks with unregulated voltages from 2.7 V to 5.5 V. It needs a quiescent current lower than 0.7 mA and is capable of delivering up to 30 mA to the load.

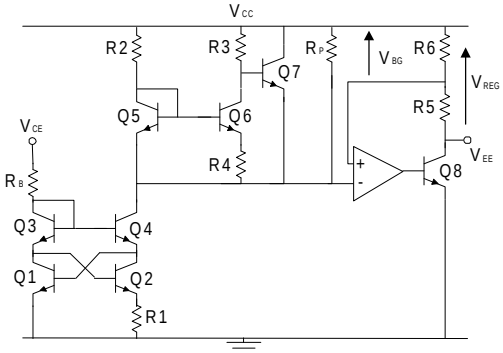

Figure 5 : Voltage regulator

EXPERIMENTAL RESULTS

The receiver has been implemented by using a high performance bipolar technology of ST which provides trench isolation, and poly-emitter NPN bipolar transistors with minimum emitter feature size of 0.4 μm and maximum transition frequency of 20 GHz.

A chip photo is shown in Fig. 6. The chip has been packaged in a TQFP44 using minimum length bonding wires for the RF inputs. A plot of the measured VCO power spectrum is shown in Fig. 7. The phase noise at 100-kHz frequency offset is -69 dBc with a resolution bandwidth of 1 kHz that means -99 dBc/Hz.

A summary of the main electrical parameters is reported in Table I.

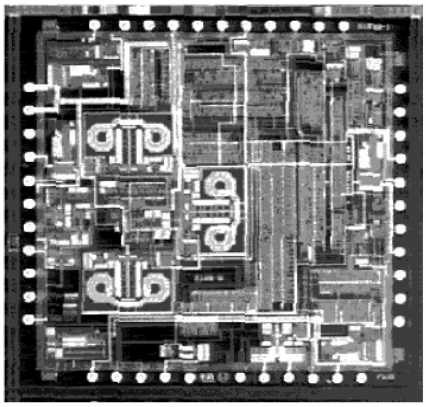

Figure 6 : Photomicrograph of the integrated receiver

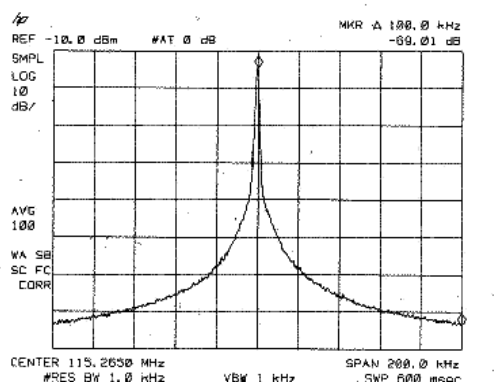

Figure 7 : Power spectrum of the VCO

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[2] G. Palmisano, M. Paparo, F. Torrisi, and P. Vita, "Noise in fully integrated PLL's," AACD'97, Advances in Analog Circuit Design, Como, Italy, April 1997.

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TABLE I

Overall Performance	
V_{CC}-V_{EE}	2.4 V
Maximum Gain	120 dB
Output Level	1 V_{PP}
I_{BIAS}	75 mA
Die Size	18 mm^2
LNA-Mixer	
Conversion gain	50 dB
Noise Figure	5 dB
Input IP3	-39 dBm
LO to RF isolation	-60 dB
RF PLL	
Loop Bandwidth	2 kHz
Phase Noise fosc=1.35 GHz, Δf=100 kHz	-99 dBc/Hz
Spurious Rejection	64 dBc